RECEIVED
CENTRAL FAX CENTER
OCT 16 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled).

2. (Canceled).

3. (Canceled).

4. (Canceled).

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Currently Amended) A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions; and

element isolation insulating films completely filling said trenches such that said trenches are filled completely with insulating films by polishing an insulating layer formed over said trenches and said semiconductor substrate such that said element isolation insulating films serve as element isolation regions,

wherein said dummy regions are formed at a scribing area with a number, size and layout so as to planarize a surface of said element isolation insulating films filled in said trenches at said scribing area by said polishing.

12. (Previously Presented) A semiconductor integrated circuit device according to claim 11, wherein a length of each of said dummy regions is shorter than a distance between external terminals.

13. (Currently Amended) A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions; and

insulating films completely filling said trenches such that said trenches are filled completely with insulating films by polishing an insulating layer formed over said trenches and said semiconductor substrate such that said insulating films serve as element isolation insulating films;

wherein said dummy regions are formed at a scribing area with a number, size and layout so as to planarize a surface of said insulating films filled in said trenches at said scribing area by said polishing.

14. (Previously Presented) A semiconductor integrated circuit device according to claim 13, wherein a length of each of said dummy regions is shorter than a distance between bonding pads.

15. (Currently Amended) A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions; and

element isolation insulating films completely filling said trenches such that said trenches are filled completely with insulating films by polishing an insulating layer formed over said trenches and said semiconductor substrate,

wherein said dummy regions are formed at a scribing area with a number, size and layout so as to planarize a surface of said insulating films filled in said trenches at said scribing area by said polishing.

16. (Previously Presented) A semiconductor integrated circuit device according to claim 15, wherein a length of each of said dummy regions is shorter than a distance between external terminals.

17. (Currently Amended) A semiconductor integrated circuit device comprising:

a trench formed in a semiconductor substrate and defining active regions and dummy regions; and

an element isolation insulating film completely filling said trench such that said trench is filled completely with insulating film by polishing an insulating film formed over said trench and said semiconductor substrate such that said element isolation insulating film serve as element isolation region,

wherein said dummy regions are formed at a scribing area with a number, size and layout so as to planarize a surface of said element isolation insulating film filled in said trench at said scribing area by said polishing.

18. (New) A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions; and

element isolation insulating films completely filling said trenches such that said trenches are filled completely with insulating films by polishing an insulating layer formed over said trenches and said semiconductor substrate such that said element isolation insulating films serve as element isolation regions,

wherein said dummy regions are formed at a scribing area with a number, size and layout so that a surface of said element isolation insulating films filled in said trenches at said scribing area has a planarized surface, said planarized surface being provided by said polishing and by said number, size and layout of dummy regions.

19. (New) A semiconductor integrated circuit device according to claim 18, wherein a length of each of said dummy regions is shorter than a distance between external terminals.

20. (New) A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions; and

insulating films completely filling said trenches such that said trenches are filled completely with insulating films by polishing an insulating layer formed over said trenches and said semiconductor substrate such that said insulating films serve as element isolation insulating films;

wherein said dummy regions are formed at a scribing area with a number, size and layout so that a surface of said insulating films filled in said trenches at said

scribing area has a planarized surface, said planarized surface being provided by said polishing and by said number, size and layout of dummy regions.

21. (New) A semiconductor integrated circuit device according to claim 20, wherein a length of each of said dummy regions is shorter than a distance between bonding pads.

22. (New) A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions; and

element isolation insulating films completely filling said trenches such that said trenches are filled completely with insulating films by polishing an insulating layer formed over said trenches and said semiconductor substrate,

wherein said dummy regions are formed at a scribing area with a number, size and layout so that a surface of said insulating films filled in said trenches at said scribing area has a planarized surface, said planarized surface being provided by said polishing and by said number, size and layout of dummy regions.

23. (New) A semiconductor integrated circuit device according to claim 22, wherein a length of each of said dummy regions is shorter than a distance between external terminals.

24. (New) A semiconductor integrated circuit device comprising:

a trench formed in a semiconductor substrate and defining active regions and dummy regions; and

an element isolation insulating film completely filling said trench such that said trench is filled completely with insulating film by polishing an insulating film formed over said trench and said semiconductor substrate such that said element isolation insulating film serve as element isolation region,

wherein said dummy regions are formed at a scribing area with a number, size and layout so that a surface of said element isolation insulating film filled in said trench at said scribing area has a planarized surface, said planarized surface being provided by said polishing and by said number, size and layout of dummy regions.